CLAIMS:

1. A method of forming a gated semiconductor assembly, comprising:

forming a silicon nitride layer over and contacting against a floating gate; and

forming a control gate over the silicon nitride layer.

2. The method of claim 1 further comprising:

forming a silicon dioxide layer over the silicon nitride layer; and

forming the control gate over the silicon dioxide layer.

3. A method of forming a gated semiconductor assembly, comprising:

forming a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having less electrical resistance than the second portion; and

forming a transistor gate over the silicon nitride layer.

4. The method of claim 3 further comprising:

forming a floating gate layer over the substrate; and

forming the silicon nitride layer over the floating gate layer.

5. The method of claim 3 further comprising:

forming a floating gate layer over the substrate;

forming the silicon nitride layer over the floating gate layer; and

patterning the floating gate layer and the silicon nitride layer into a floating gate shape.

6. The method of claim 3 wherein the second portion of the silicon nitride layer is over the first portion, the method further comprising:

forming a silicon dioxide layer over said second portion; and

forming the control gate over the silicon dioxide layer.

7. The method of claim 6 wherein the forming the silicon dioxide layer comprises growing the silicon dioxide from silicon of the second portion of the silicon nitride layer.

8. The method of claim 3 wherein the silicon nitride layer comprises at least one sidewall, and wherein the second portion is over the first portion, the method further comprising:

forming a silicon dioxide layer over said second portion and along the at least one sidewall of the silicon nitride layer; and

forming the transistor gate over the silicon dioxide layer.

9. The method of claim 8 wherein the forming the silicon dioxide layer comprises growing the silicon dioxide from silicon of the first and second portions of the silicon nitride layer.

10. The method of claim 3 wherein the forming the silicon nitride layer comprises:

chemical vapor depositing the first portion utilizing a first mixture having a first ratio of a silicon precursor gas to a nitrogen precursor gas; and

chemical vapor depositing the second portion utilizing a second mixture having a second ratio of the silicon precursor gas to the nitrogen precursor gas, the first ratio being greater than the second ratio.

11. The method of claim 10 wherein the chemical vapor depositings of the first and second portions occur in a common and uninterrupted deposition process.

12. A method of forming a gated semiconductor assembly, comprising:

forming a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion and a second portion displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion; and

forming a gate over the silicon nitride layer.

13. The method of claim 12 further comprising incorporating the gate into one of an EPROM or EEPROM device as a control gate.

14. A method of forming a gated semiconductor assembly, comprising:

forming a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion; and

forming a transistor gate over the silicon nitride layer.

15. The method of claim 14 wherein the second portion of the silicon nitride layer is over the first portion, the method further comprising:

forming a silicon dioxide layer over said second portion; and

forming the transistor gate over the silicon dioxide layer.

16. The method of claim 15 wherein the forming the silicon dioxide layer comprises growing the silicon dioxide from silicon of the second portion of the silicon nitride layer.

17. The method of claim 14 wherein the silicon nitride layer comprises at least one sidewall, and wherein the second portion is over the first portion, the method further comprising:

forming a silicon dioxide layer over said second portion and along the at least one sidewall of the silicon nitride layer; and

forming the transistor gate over the silicon dioxide layer.

18. The method of claim 17 wherein the forming the silicon dioxide layer comprises growing the silicon dioxide from silicon of the first and second portions of the silicon nitride layer.

19. A method of forming a gated semiconductor assembly, comprising:

forming a floating gate layer over a substrate;

forming a silicon nitride layer over the floating gate layer, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion; and

forming a control gate over the silicon nitride layer.

20. The method of claim 19 further comprising:

forming a silicon dioxide layer over the substrate; and

forming the floating gate layer over the silicon dioxide layer.

21. The method of claim 19 further comprising patterning the floating gate layer into a floating gate shape after forming the silicon nitride layer.

22. The method of claim 19 wherein the forming the silicon nitride layer comprises:

chemical vapor depositing the first portion utilizing a first mixture having a first ratio of a silicon precursor gas to a nitrogen precursor gas; and

chemical vapor depositing the second portion utilizing a second mixture having a second ratio of the silicon precursor gas to the nitrogen precursor gas, the first ratio being greater than the second ratio.

23. The method of claim 22 wherein the chemical vapor depositing the first portion occurs before the chemical vapor depositing the second portion.

24. The method of claim 22 wherein the chemical vapor depositing the first portion and the chemical vapor depositing the second portion occur in a common and uninterrupted deposition process.

25. The method of claim 22 wherein the floating gate layer comprises polycrystalline silicon.

26. The method of claim 22 wherein the forming the floating gate layer comprises:

chemical vapor depositing amorphous silicon; and

thermally treating the amorphous silicon to form polycrystalline silicon.

27. The method of claim 19 wherein the floating gate layer comprises at least one of amorphous silicon and polycrystalline silicon, and wherein the forming the floating gate layer and the forming the silicon nitride layer occur in a common and uninterrupted chemical vapor deposition process.

28. The method of claim 19 further comprising:

forming a silicon dioxide layer over the substrate;

forming the floating gate layer over the silicon dioxide layer, the floating gate layer comprising at least one of amorphous silicon and polycrystalline silicon;

forming the first portion of the silicon nitride layer by chemical vapor depositing utilizing a first mixture having a first ratio of a silicon precursor gas to a nitrogen precursor gas; and

forming the second portion of the silicon nitride layer over the first portion by chemical vapor depositing utilizing a second mixture having a second ratio of the silicon precursor gas to the nitrogen precursor gas, the first ratio being greater than the second ratio, the chemical vapor depositing the first portion and the chemical vapor depositing the second portion occurring in a common and uninterrupted deposition process;

after forming the first and second portions of the silicon nitride layer, forming a patterned photoresist layer over and against the second portion of the silicon nitride layer;

transferring a pattern from the patterned photoresist layer to the polycrystalline silicon and the first and second portions of the silicon nitride layer to form a stack comprising the patterned floating gate layer and the patterned first and second portions of the silicon nitride layer, the stack having at least one sidewall;

growing a silicon dioxide layer over the second portion and along the at least one sidewall of the stack; and

forming the control gate over the silicon dioxide layer.

29. The method of claim 28 wherein the patterned photoresist layer is formed against the silicon nitride layer, wherein the patterned photoresist is formed by exposing a photoresist material to light, and wherein the silicon nitride layer is utilized as an antireflective material during the exposure of the photoresist material to light.

30. A method of forming a semiconductor assembly, comprising:

forming a first material layer over a substrate;

forming a silicon nitride layer over the first material layer, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion;

forming a photoresist layer over the silicon nitride layer;

patterning the photoresist layer, the patterning comprising exposing portions of the layer of photoresist to light and utilizing the silicon nitride layer as an antireflective material during the exposing; and

transferring the pattern from the patterned photoresist to the silicon nitride layer and the first material layer.

31. The method of claim 30 wherein the first material layer comprises at least one of polycrystalline silicon and amorphous silicon.

32. The method of claim 30 wherein the forming the silicon nitride layer comprises:

chemical vapor depositing the first portion utilizing a first mixture having a first ratio of a silicon precursor gas to a nitrogen precursor gas; and

chemical vapor depositing the second portion utilizing a second mixture having a second ratio of the silicon precursor gas to the nitrogen precursor gas, the first ratio being greater than the second ratio.

33. The method of claim 32 wherein the chemical vapor depositing the first portion and the chemical vapor depositing the second portion occur in a common and uninterrupted deposition process.

34. A gated semiconductor assembly, comprising:

a silicon nitride layer over and contacting against a floating gate; and

a control gate over the silicon nitride layer.

35. The gated semiconductor assembly of claim 34 further comprising a silicon dioxide layer between the silicon nitride layer and the control gate.

36. A gated semiconductor assembly, comprising:

a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having less electrical resistance than the second portion; and

a gate over the silicon nitride layer.

37. The gated semiconductor of claim 36 wherein the gate is a control gate of an EPROM or an EEPROM device.

38. The gated semiconductor of claim 36 further comprising:

the second portion of the silicon nitride layer being over the first portion;

a silicon dioxide layer over said second portion; and

the control gate being over the silicon dioxide layer.

39. A gated semiconductor assembly comprising:

a silicon nitride layer over a substrate, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion; and

a transistor gate over the silicon nitride layer.

40. The gated semiconductor of claim 39 further comprising:

the second portion of the silicon nitride layer being over the first portion;

a silicon dioxide layer over said second portion; and

the transistor gate being over the silicon dioxide layer.

41. A gated semiconductor assembly comprising:

a substrate;

a polycrystalline silicon layer over the substrate;

a silicon nitride layer over the polycrystalline silicon layer, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion; and

a control gate over the silicon nitride layer.

42. The gated semiconductor of claim 41 wherein the first portion is over the second portion.

43. The gated semiconductor of claim 41 wherein the second portion is over the first portion.

44. A gated semiconductor assembly comprising:

a substrate;

a floating gate over the substrate;

a control gate over the floating gate; and

an electron barrier layer between the floating gate and the control gate, the electron barrier layer comprising a silicon nitride layer, the silicon nitride layer comprising a first portion and a second portion elevationally displaced from the first portion, the first portion having a greater stoichiometric amount of silicon than the second portion.

45. The gated semiconductor of claim 44 wherein the first portion is over the second portion.

46. The gated semiconductor assembly of claim 44 wherein the electron barrier layer further comprises a silicon dioxide layer between the control gate and the silicon nitride layer.

47. The gated semiconductor assembly of claim 44 wherein the floating gate comprises polycrystalline silicon and has at least one sidewall, and wherein the silicon nitride layer has at least one sidewall, the assembly further comprising a layer of dioxide extending along said sidewalls of the silicon nitride layer and the polycrystalline silicon.